AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

LISTING OF CLAIMS

1. (ORIGINAL) A method of forming a nickel silicide layer on an exposed silicon surface comprising:

depositing a nickel alloy layer on the exposed silicon surface, the nickel alloy including nickel and an alloying metal;

reacting the nickel alloy layer with the exposed silicon surface to form a nickel silicide layer having an upper layer and a lower layer, wherein the alloying metal is preferentially segregated in the upper layer.

2. (ORIGINAL) A method of forming a nickel silicide layer according to claim 1, wherein:

the lower layer includes at least 95 atomic percent nickel and silicon.

3. (ORIGINAL) A method of forming a nickel silicide layer according to claim 2, wherein:

the lower layer includes at least 99 atomic percent nickel and silicon.

4. (ORIGINAL) A method of forming a nickel silicide layer according to claim 3, wherein:

the nickel and silicon are present in the lower layer in an atomic ratio of about 1.

5. (ORIGINAL) A method of forming a nickel silicide layer according to claim 1, further comprising:

forming a capping layer on the nickel alloy layer before reacting the nickel alloy with the exposed silicon.

6. (PREVIOUSLY PRESENTED) A method of forming a nickel silicide layer according to claim 5, wherein: the capping layer includes a major portion of titanium nitride.

7. (ORIGINAL) A method of forming a nickel silicide layer according to claim 1, wherein: the alloying metal is at least one metal selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium, niobium and combinations thereof, and constitutes no more than about 10 atomic percent of the nickel alloy.

8. (ORIGINAL) A method of forming a nickel silicide layer according to claim 1, wherein:

the alloying metal is tantalum and is present in a concentration of between about 0.1 and about 10 atomic percent of the nickel alloy.

9. (ORIGINAL) A method of forming a nickel silicide layer according to claim 8, wherein:

the nickel alloy consists essentially of nickel and tantalum, the tantalum being present in an amount between about 0.1 and about 5 atomic percent.

10. (ORIGINAL) A method of forming a nickel silicide layer according to claim 5, wherein: the capping layer has a nitrogen:titanium atomic ratio of at least about 0.5.

11. (ORIGINAL) A method of forming a nickel silicide layer according to claim 6, wherein: the lower layer has a first thickness; and

the upper layer has a second thickness, wherein the first thickness is at least 70% of a sum of the first thickness and the second thickness.

12. (ORIGINAL) A method of forming a nickel silicide layer according to claim 6, wherein: the lower layer has a first thickness; and

the upper layer has a second thickness, wherein the first thickness is at least 85% of a sum of the first thickness and the second thickness.

13. (ORIGINAL) A method of forming a nickel silicide layer according to claim 12, wherein: the lower layer has a tantalum concentration no greater than about 4.9 atomic percent; and

the upper layer has a tantalum concentration of at least about 5 atomic percent.

14. (ORIGINAL) A method of forming a nickel silicide layer according to claim 12, wherein: the lower layer has a tantalum concentration no greater than about 0.5 atomic percent; and

the upper layer has a tantalum concentration no greater than about 60 percent.

15. (ORIGINAL) A method of manufacturing a semiconductor device comprising: defining an active region on a semiconductor substrate; forming a gate electrode in the active region;

exposing a silicon surface on the semiconductor substrate;

forming a nickel alloy layer on the semiconductor substrate, the nickel alloy including nickel and an alloying metal;

reacting a portion of the nickel alloy layer with the exposed silicon surface to form a nickel silicide region; and

removing an unreacted portion of nickel alloy layer from the semiconductor substrate;

wherein the nickel silicide region includes an upper layer and a lower layer, and further wherein the alloying metal is preferentially segregated into the upper layer.

16. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

nickel and silicon represent at least about 95 atomic percent of the lower layer of the nickel silicide region.

17. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 16, wherein:

nickel and silicon represent at least about 99 atomic percent of the lower layer of the nickel silicide region.

18. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the lower layer of the nickel silicide region includes nickel atoms and silicon atoms in a ratio of between about 9:10 and 10:9.

19. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, further comprising:

forming a capping layer on the nickel alloy layer;

maintaining the capping layer until the nickel silicide region has been formed; and removing the capping layer.

20. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 18, wherein:

the capping layer includes a major portion of TiN.

21. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein exposing the silicon surface on the semiconductor substrate includes:

exposing portions of the semiconductor substrate in a source/drain region formed in the active region.

22. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, further comprising:

forming a gate capping layer on the gate electrode to protect an upper surface of a polysilicon layer included in the gate electrode.

23. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein exposing silicon surfaces on the semiconductor substrate includes:

exposing silicon surfaces only on the gate electrode.

24. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 23, further comprising:

forming an insulating layer on the semiconductor substrate and the gate electrode; and

removing an upper portion of the insulating layer to expose a silicon surface on the gate electrode with a lower portion of the insulating layer covering source/drain regions formed in the active region.

25. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein exposing silicon surfaces on the semiconductor substrate includes:

exposing silicon surfaces in source/drain regions formed in the active region; and exposing a silicon surface on the gate electrode.

26. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the alloying metal is at least one metal selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium, niobium and combinations thereof, and constitutes no more than about 10 atomic percent of the nickel alloy.

27. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 26, further comprising:

forming a capping layer on the nickel alloy layer;

maintaining the capping layer until the nickel silicide region has been formed; and

removing the capping layer.

28. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the alloying metal consists essentially of tantalum and constitutes no more than about 10 atomic percent of the nickel alloy; and

29. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 28, wherein:

tantalum constitutes no more than about 5 atomic percent of the nickel alloy.

30. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein reacting the nickel alloy with the exposed silicon surfaces to form nickel silicide regions on the semiconductor substrate includes:

heating the substrate and the nickel alloy layer to a temperature between about 250°C. and about 550°C. for a silicidation period of between about 10 seconds and about 30 minutes.

31. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, further comprising:

completing the manufacture of the semiconductor device utilizing processes such that at least about 90 percent of the nickel silicide region remains nickel monosilicide, NiSi.

32. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 31, wherein:

the nickel silicide region contains substantially no nickel disilicide, NiSi.sub.2.

33. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the lower layer has a first thickness;

the upper layer has a second thickness; and

the first thickness is at least 70% of a sum of the first thickness and the second thickness.

34. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the lower layer has a first thickness;

the upper layer has a second thickness; and

the first thickness is at least 85% of a sum of the first thickness and the second thickness.

35. (WITHDRAWN) A semiconductor device comprising:

a semiconductor substrate, the semiconductor substrate including an active area and an isolation area;

a gate electrode structure formed in the active area, the gate electrode structure including an insulating layer formed on the active area and a conductive layer formed on the insulating layer;

first and second doped regions, the doped regions formed in the active area and separated by the gate electrode structure; and

a nickel silicide region on the first and the second doped region and on the gate electrode structure, the nickel silicide region having a lower layer and an upper layer, the lower layer having a first thickness T_1 and a first alloying metal concentration C_{AM1} and the upper layer having a second thickness T_2 and a second alloying metal concentration C_{AM2}.

36. (WITHDRAWN) A semiconductor device comprising:

a semiconductor substrate, the semiconductor substrate including an active area and an isolation area;

a gate electrode structure formed in the active area, the gate electrode structure including an insulating layer formed on the active area and a conductive layer formed on the insulating layer;

first and second doped regions, the doped regions formed in the active area and separated by the gate electrode structure; and

a nickel silicide region on the first and the second doped region, the nickel silicide region having a lower layer and an upper layer, the lower layer having a first thickness T_1 and a first alloying metal concentration C_{AM1} and the upper layer having a second thickness T_2 and a second alloying metal concentration C_{AM2}.

37. (WITHDRAWN) A semiconductor device comprising:

a semiconductor substrate, the semiconductor substrate including an active area and an isolation area;

a gate electrode structure formed in the active area, the gate electrode structure including an insulating layer formed on the active area and a conductive layer formed on the insulating layer;

first and second doped regions, the doped regions formed in the active area and separated by the gate electrode structure; and a nickel silicide region on the gate structure, the nickel silicide region having a lower layer and an upper layer, the lower layer having a first thickness T_1 and a first alloying metal concentration C_{AM1} and the upper layer having a second thickness T_2 and a second alloying metal concentration C_{AM2}.

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